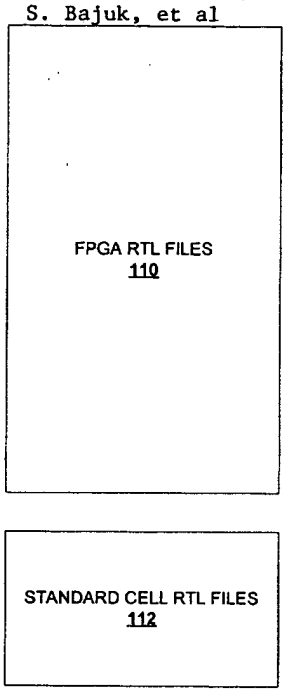


FIGURE 1A
(PRIOR ART)

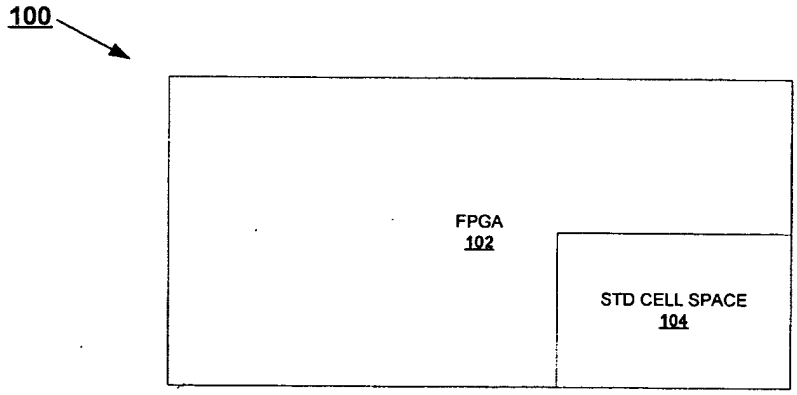


FIGURE 1B

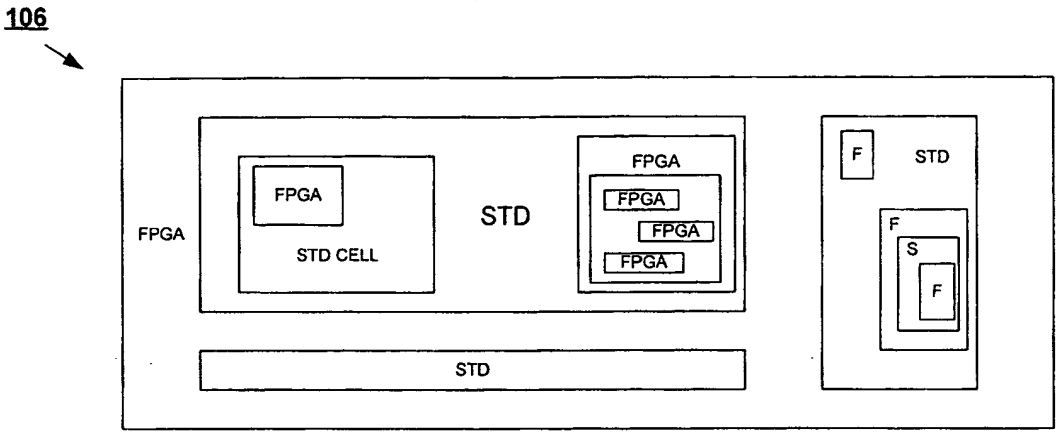


FIGURE 1C

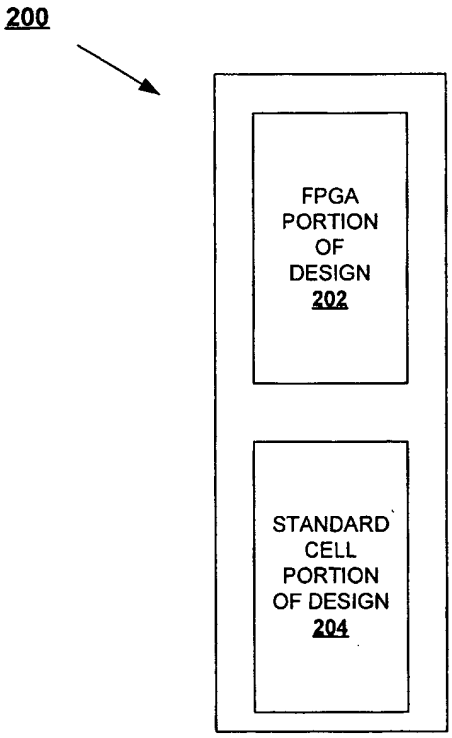
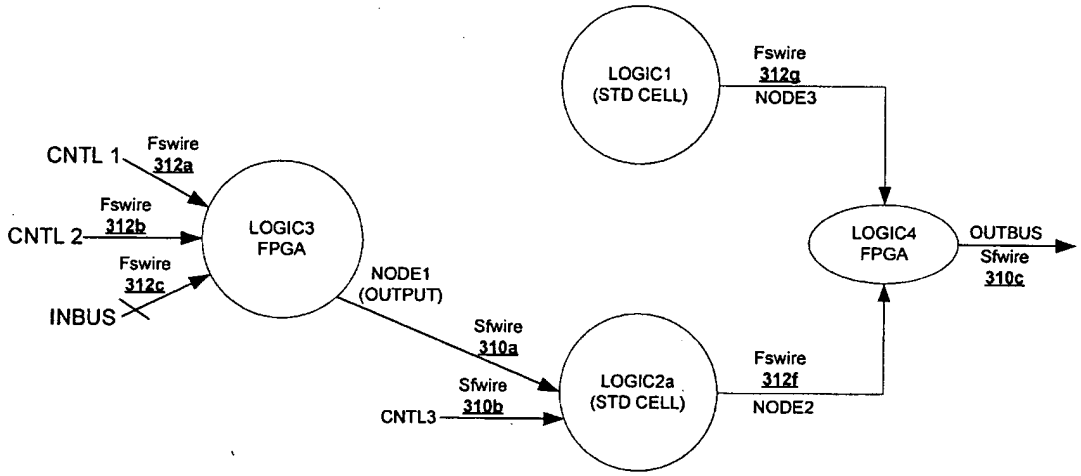


FIGURE 2

	WIRE TYPE	MEANING	FIXED OR ADJUSTABLE
302	(S)wire	STANDARD CEL	FIXED
304	Fwire	FPGA	FIXED
306	sFwire	TOOL REPARTITION REQUEST: FPGA -> **STD CELL**	ADJUSTABLE
308	fSwire	TOOL REPARTITION REQUEST: STD CELL -> **FPGA**	ADJUSTABLE
310	Sfwire	**STANDARD CELL**, ACCEPTED BY DESIGNER	ADJUSTABLE
312	Fswire	**FPGA**, ACCEPTED BY DESIGNER	ADJUSTABLE

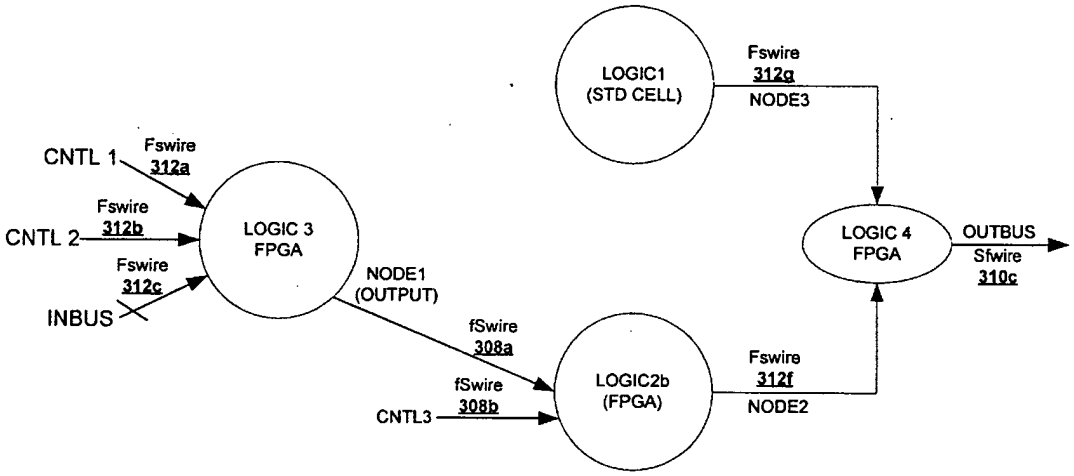
FIGURE 3



EXAMPLE VERILOG

```
module MyDesign (CNTL1, CNTL2, INBUS, CNTL3,
OUTBUS);
input Fswire CNTL1, CNTL2;
input Fswire [7:0] INBUS;
input Sfwire CNTL3;
Sfwire NODE1;
Fswire NODE2, NODE3;
output Sfwire [7:0] OUTBUS;
```

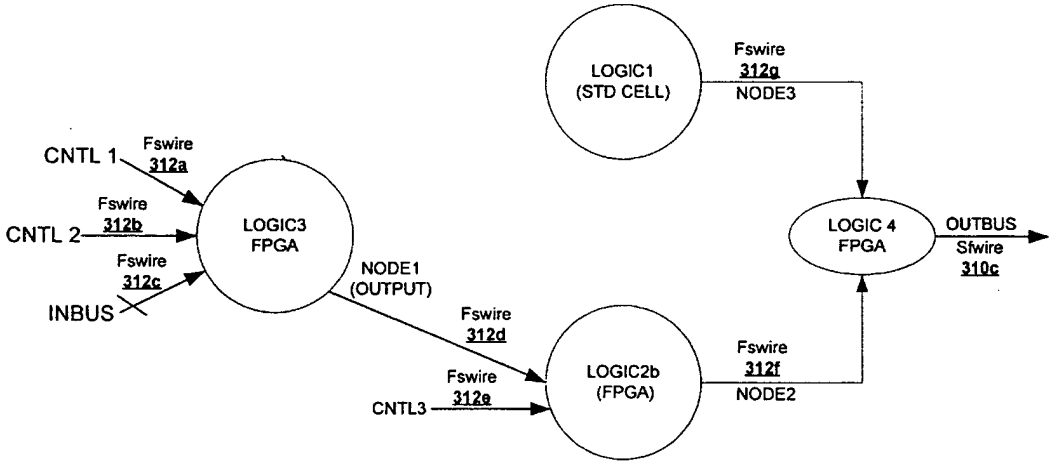
FIGURE 4A



EXAMPLE VERILOG

```
module MyDesign (CNTL1, CNTL2, INBUS, CNTL3,
OUTBUS);
input Fswire CNTL1, CNTL2;
input Fswire [7:0] INBUS;
input fSwire CNTL3;
fSwire NODE1;
Fswire NODE2, NODE3;
output Sfwire [7:0] OUTBUS;
```

FIGURE 4B



EXAMPLE VERILOG

```
module MyDesign (CNTL1,CNTL2, INBUS, CNTL3,
OUTBUS);
input Fswire CNTL1, CNTL2;
input Fswire [7:0] INBUS;
input Fswire CNTL3;
Fswire NODE1;
Fswire NODE2, NODE3;
output Sfwire [7:0] OUTBUS;
```

FIGURE 4C

OPTIONS FOR PARTITIONING A STANDARD CELL WIRE

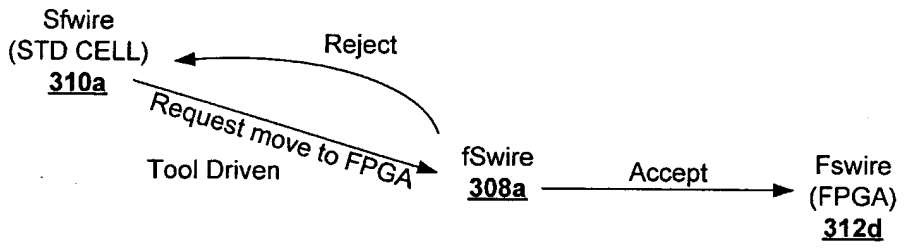


FIGURE 5A

OPTIONS FOR PARTITIONING A STANDARD CELL WIRE

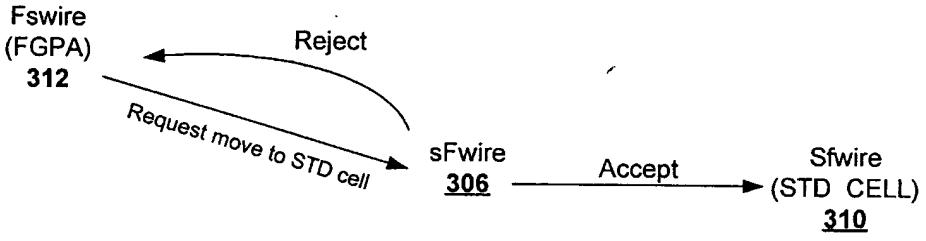


FIGURE 5B

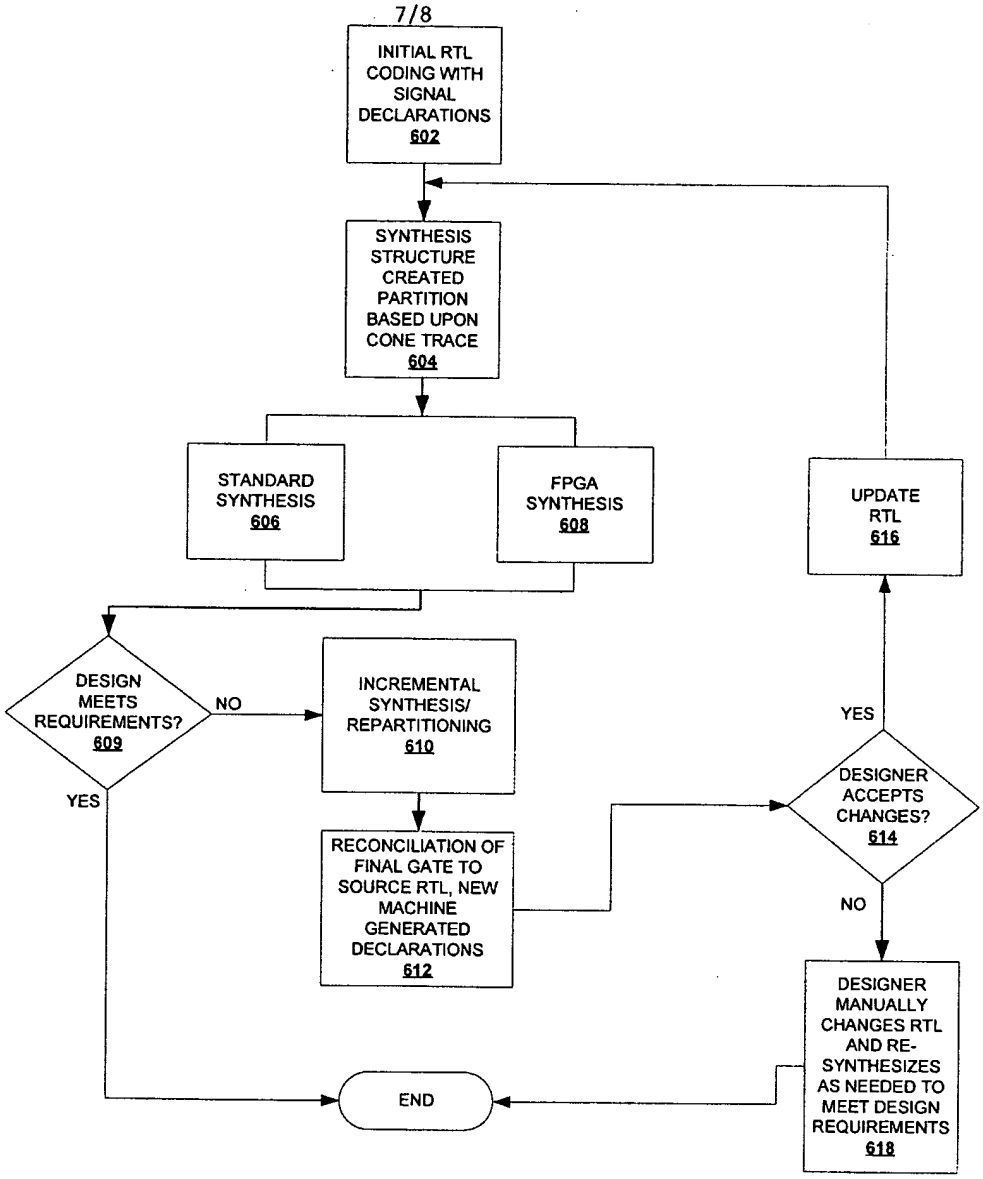

INITIAL RTL CODING WITH SIGNAL DECLARATIONS 602
SYNTHESIS STRUCTURE CREATED PARTITION BASED UPON CONE TRACE 604
STANDARD SYNTHESIS 606
FPGA SYNTHESIS 608
DESIGN MEETS REQUIREMENTS? 609
NO
YES
INCREMENTAL SYNTHESIS/ REPARTITIONING 610
RECONCILIATION OF FINAL GATE TO SOURCE RTL, NEW MACHINE GENERATED DECLARATIONS 612
DESIGNER ACCEPTS CHANGES? 614
YES
NO
UPDATE RTL 616
DESIGNER MANUALLY CHANGES RTL AND RE-SYNTHESIZES AS NEEDED TO MEET DESIGN REQUIREMENTS 618
END

FIGURE 6

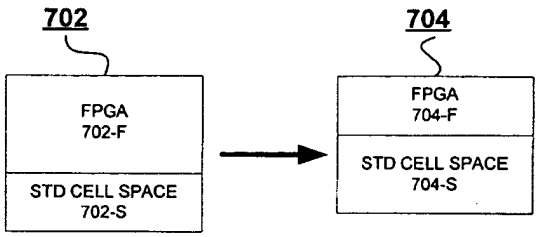


FIGURE 7A

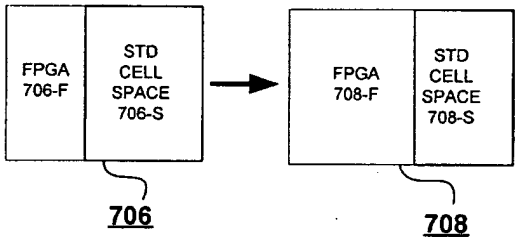


FIGURE 7B